Consider the following state diagram:

![State Diagram]

Legend: $Q_A, Q_B$

There is one input ($D$) and no outputs. The circuit goes to state $11$ when the input is high for three or more successive clock pulses. It can be used to detect a sequence of three or more $1$'s in an input data stream by decoding the state $11$. The circuit is to be implemented using two JK flip-flops plus combinatorial circuitry as indicated below. Design the combinatorial circuits for $J_A$ and $K_A$. Be reasonably efficient.

Skeleton of circuit: (combinatorial circuitry not shown)

![Circuit Diagram]