# PRELIMINARY COURSE OUTLINE

## Physics 116B Winter 2004

Introduction to Digital Electronics

**Class meets** MWF 1:10-2:00 PM in 158 Roessler

**Lab meets** M or W 3:10-6:00 PM in 152 Roessler.

<table>
<thead>
<tr>
<th>Week</th>
<th>Monday</th>
<th>Topics/Notes</th>
<th>Lab</th>
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<tbody>
<tr>
<td>1</td>
<td>(Jan 5)</td>
<td>Intro; comparator, Schmitt trigger, etc.</td>
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<td><strong>First day of class</strong> is Wednesday, Jan. 7</td>
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<td>2</td>
<td>Jan 12</td>
<td>Pulse circuit analysis; Laplace transform</td>
<td>10: Schmitt Trigger</td>
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| 3    | Jan 19 | *M.L. King holiday on Monday*  
Logic gates and Boolean algebra | 11: Relaxation Oscillator  
*(Mon. lab meets Friday)* |
| 4    | Jan 26 | Combinational circuit design  
Logic circuits: TTL, CMOS, ECL | 12: Combinational logic |
| 5    | Feb 2  | Flip-flops and counters  
**Exam 1** on Wednesday, Feb. 4 | 13: Inside Digital IC’s |
| 6    | Feb 9  | Sequential circuits | 14: Sequential Logic |
| 7    | Feb 16 | *Presidents’ Day holiday on Monday*
*Now Wed. lab starts sequence*
A to D, D to A conversion | 15: Analog to Digital and Digital to Analog Conversion  
*(also following Monday)* |
| 8    | Feb 23 | M68000 Microcomputer,  
Assembly Language, I/O | 16: Tristate Busses and Memory |
| 9    | Mar 1  | **Exam 2** on Wednesday, March 3 | 17: M68000 Assembly Language |
| 10   | Mar 8  | Intro. to discrete signal analysis and FFT | 18: Basic M68000 I/O  
*(via SCSI Port)* |
| 11   | Mar 15 | **Last 116B class** is Monday, March 15 | **(Monday lab does Lab 18)** |

**Final Exam:** Tuesday, March 23, 10:30 AM - 12:30 PM
Instructor: David Pellett
Office: Rm. 337 Physics
Office Hours: W 11:30-12:30 in Rm 152 Physics or by appointment.
E-mail: pellett@physics.ucdavis.edu
Telephone: (530) 752-1783

Lab TA: Joe Davies
Office: Rm. 434 Physics
E-mail: davies@physics.ucdavis.edu
Office Hours: TBA

Text:
Bobrow, Fundamentals of Electrical Engineering, 2nd ed.

References:
Ford and Topp, Macintosh Assembly System (lab copies to loan)
Motorola, M68000 Family Microprocessor User’s Manual
Motorola, M68000 Family Programmer's Reference Manual
plus library references and supplementary handouts

Grading: 18% MT1, 18% MT2, 25% Lab(required, on time), 10% HW, 29% Final.

Assignment 1, due Wednesday, 1/14/04:
Read Bobrow, Ch. 10: Sec. 10.5; review Ch. 3 (response of circuits to pulses: particularly secs 3.3 and 3.4); Ch. 5: 5.5-5.7 (Laplace transform circuit analysis).
Problems: Ch. 10: 10.67, 10.72, 10.77(a), 3.28 (assume the voltage across the capacitor is 12 V and the current through it is 0 just before the switch is opened), 3.42 (assume the voltage across the capacitor and the current through it are zero just before the pulse arrives; you can use Thevenin's theorem here for the voltage source and two resistors).