Diagrams from Horowitz and Hill show connections of an input register and an output register to an M68008 microprocessor.

(a) Make a timing diagram showing the clock signal on the 74LS574 octal D latch when the output register is accessed with its valid address during a write cycle. Also show the output of the address decoder. Fill these two signals in on the copy of the write cycle timing diagram which shows $R/W$, the $\overline{DS}$ signal, VALID ADDRESS on the address lines and VALID DATA on the data lines (lumped together as usual). (i.e., use Figure below)

(b) Explain why the output register can have its tri-state output lines enabled continuously without causing conflicts with the computer data bus.