Logic circuits & how they work

1. Evolution from RTL inverter to DTL NAND to TTL NAND (and Schottky TTL).

BJT as switch - cutoff or saturation (discussed earlier)

For example (not TTL levels)
\[ \text{Vin low means } \leq 0.2 \text{V} \]
\[ \text{Vin high means } \geq 2 \text{V} \]

If \( \text{Vin = 0.2V} \), \( \text{VBE < 0.5V} \)
BJT is cut off, \( \text{Vout = 5V} \)

If \( \text{Vin} \geq 2\text{V} \), the transistor is in saturation,
\( \text{VB} \approx 0.8\text{V}, \text{Vout} = 0.2\text{V} \)
acting as logic inverter

DTL NAND gate uses diodes to form logic (Fig. 7.26 in text)

If either \( V_1 \) or \( V_2 \)
is at 0.2V,
\( V_B = 0.9\text{V} \), not enough to turn BJT on

(E.g., if \( V_1 = 0.3 \), \( V_2 = 5\text{V} \)
\( D_2 \) is reverse biased, bar \( D_0 \) pulls BJT input down.)

If both \( V_1 \) and \( V_2 \) are +5V

\( D_3 \) and \( D_4 \) are used to increase the turn-on threshold at the input due to their forward voltage drop.

\[ \text{F = AB} \]
\[ \begin{array}{c|c|c}
0 & 0 & 0 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array} \]

( NAND)
**Improvement to make TTL worse**

To omit pole output and transistor input replacing diodes \(E_7, \text{p}32\). Relation between \(V_{out}, V_1, V_2\) is the same.

Gives more drive current in the high state and faster response.

\[\text{start here}\]

Lower impedance path in high state than RTL or DTL.

Changes through \(Q_4, D\) and \(100 \Omega\) in high state

Load capacitaional

**Totem Pole output stage**

\(Q_2\) controls \(Q_1\) and \(Q_3\)

\(Q_2\) on: \(Q_1\) off, \(Q_3\) off.

\(\Rightarrow\) output high

\(Q_2\) off:

\[V_{CE2} = 0.2\] (saturation)

\[V_{B3} = 0.8\] (saturation)

\[V_{B4} = V_{CE} = 1.0V\]

\[V_{out} = 0.2V\] (output)

The forward voltage drop across \(D\) is big enough to keep \(V_{BE4} < 0.5V\) (off)

\[V_{BE4} + V_D = 1 - 0.2 = 0.8V\]

\(<\) sum of cut-in voltage

Note the parallel (to DTL)

BJT provides current gain, an advantage over DTL.

Note unconventional "reverse active" mode when \(V_1\) and \(V_2\) are both high.

\(V_1, V_2\) low \(\Rightarrow ICQ1 > 0, Q_2\) off \(\Rightarrow\) output high

\(V_1\) and \(V_2\) high \(\Rightarrow ICQ1 < 0, Q_2\) on \(\Rightarrow\) output low

\(Y = \overline{A} + B = \overline{A}B\) (see prob. handout)
Saturation may lead to long storage time, slowing BJT "off" transition (base region flooded with minority carriers; slowly diffuse out & be depletion region). Prevent saturation with Schottky diode.

- Metal-semiconductor junction - majority carrier device.
- Forward voltage drop 0.4 V rather than 0.7 V.
- Use to prevent BJT base-collector diode from being forward biased, prevent saturation.

**Schottky Barrier**
- N⁺ ohmic contact
- Al / n⁺-type Si:
  - lightly doped

**Forward bias reduces the net field, raising the Ec level in the bulk, more electrons get over from semiconductor there is a depletion region, but there are no minority carriers.**

For Schottky contact, use heavy doping, get tunneling through a narrow barrier (Ef within 3kT of Ec for degenerate semiconductor).

See Table 7.3 in Bobrow

BJT remains in active region with \( V_{BC} \) limited by Schottky diode

(As Schottky TTL circuit - slightly different. See text.)
TTL CIRCUIT MODIFICATIONS TO ALLOW USE WITH DATA BUS-OUTPUT INTERCONNECTION

OPEN COLLECTOR OUTPUT:

 rest or circuit

open or closed switch to ground

(high state) (low state)

simplest case: 5

inverses

R_{pu} ← pull-up resistor, e.g. 1 kΩ

A ← a switch

b switch "output " bussed" (called "wired or" although logic may vary)

A

B

H → open collector

Y (with pull-up)

L L open open H H Y = A + B

L H open closed L L

H L closed open L L

H H closed closed L L

Advantage: Simple

Disadvantage: can be slow, depending on R value.

Two-input multiplier:

\( Y = D_1 \) if \( S = 0 \)

\( Y = D_1 \) if \( S = 1 \)

\( Y = D \) \( S + D_1 \) \( S \)

Simplified logic table:

<table>
<thead>
<tr>
<th>S</th>
<th>D1</th>
<th>D0</th>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

X = "don't care"
Tri-state output:

3 possibilities: 0, 1, high impedance ("Z")

- Better way to share bus lines - active pull-up in high state, no external pull-up required.

TI circuit modification:

New emitter and diode added to provide high-Z state

OE = output enable

If OE is low, Q1 pulls the base of Q2 low, turning it off. The OE connection through the diode pulls the base of Q4 low, turning it off. Since Q2 is off, the base of Q3 is at ground, so Q3 is off. Thus the Y output is floating.

⇒ high impedance state.

If OE is high, it has no further effect on circuit operation, as you can check.

Two-input multiplexer:

Y = D1 \cdot \overline{OE} + D0 \cdot S

"0" indicates tri-state output.
n-MOS and p-MOS transistors as switches and CMOS inverter

(a) Enhancement mode MOSFET as inverter:

\[ V_{th} \quad V_{DD} \quad \text{See text, Fig. 8.23} \]

Approx transfer characteristics:

so if we use logic levels with \( V_L = V_{th} \) and \( V_H = V_{DD} \), this is an inverter. Model MOSFET as open switch with \( V_{in} = \text{low} \) and closed switch (although with non-negligible resistance) with \( V_{in} = \text{high} \).

(b) By symmetry, p-MOS with source hooked to \(+V_{DD}\) and drain through \( R \) to ground would be open switch with \( V_{in} = \text{high} \), closed switch (with non-negligible \( R \)) with \( V_{in} = \text{low} \). The switch is closed to \(+V_{DD}\) so output would be high with input low:

(c) CMOS inverter

\[ V_{in} \quad \ldots \quad V_{out} = \overline{A} \quad \text{with active pull-up.} \]

\( A \quad \text{n-MOS} \quad \text{p-MOS} \quad \text{Y} \)
\| \text{L} \quad \text{OFF} \quad \text{ON} \quad \text{H} \]
\| \text{H} \quad \text{ON} \quad \text{OFF} \quad \text{L} \]

(Very simple integrated circuit structure—See Text, Fig. 8.36)
CMOS NAND EXAMPLES

\[ V_{DD} \]

\[ nM_1 \]

\[ pM_2 \]

\[ M_3 \]

\[ M_4 \]

\[ B \]

\[ V_{DD} \]

\[ Y \]

\[ A \]

\[ nM_3 \]

\[ M_2 \]

\[ B \]

\[ M_4 \]

\[ \parallel \]

\[ \text{parallel} \]

\[ \text{series} \]

\[ \text{OFF} \]

\[ \text{OPEN} \]

\[ \text{ON} \]

\[ \text{CLOSED} \]

CMOS GATE

SWITCH MODEL

For variable \( A \), nMOS on for \( A \), pMOS on for \( \overline{A} \), etc.

[careful that no state results in direct short between \( V_{DD} \) and ground.]

TRUTH TABLE:  (positive logic, \( L = 0 \ V, H = V_{DD} \))

<table>
<thead>
<tr>
<th>( A )</th>
<th>( B )</th>
<th>( M_1 )</th>
<th>( M_2 )</th>
<th>( M_3 )</th>
<th>( M_4 )</th>
<th>( Y )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
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<tr>
<td>1</td>
<td>1</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>0</td>
</tr>
</tbody>
</table>

\[ Y = \overline{AB} = \overline{A} + \overline{B} \]