Logic circuits & how they work

(a) Evolution from RTL inverter to DTL NAND to TTL NAND (and Schottky TTL).

BJT as switch - cutoff or saturation (discussed earlier)

[Diagram of BJT circuit]

For example (not TTL levels)
- \( V_{in} \) low means \( <0.2V \)
- \( V_{in} \) high means \( \geq 2V \)

If \( V_{in} \leq 0.2V, V_{BE} < 0.5V \)
BJT is cut off, \( V_{out} \approx 5V \)

If \( V_{in} \geq 2V \), the transistor is in saturation,
\( V_{BE} \approx 0.7V, V_{out} \approx 0.2V \),
acting as logic inverter

DTL NAND gate uses diodes to form logic (Fig. 7.26 in text)

[Diagram of DTL NAND gate with diodes]

If either \( V_1 \) or \( V_2 \) is at 0.2,
\( V_3 = 0.9V \), not enough to turn BJT on

(E.g., if \( V_1 = 0.3, V_2 = 5V \)
\( D_2 \) is reverse biased,
bar \( D_2 \) pulls BJT input down)

If both \( V_1 \) and \( V_2 \) are +5
current flows through \( D_3 + D_4 \)
to pull \( V_{BE} \) up to 0.8V
and output goes low.

\[ \begin{array}{c|c|c|c}
0 & 0 & 0 & 0 \\
0 & 0 & 1 & 1 \\
0 & 1 & 0 & 1 \\
0 & 1 & 1 & 0 \\
1 & 0 & 0 & \overline{A} \\
1 & 0 & 1 & \overline{B} \\
1 & 1 & 0 & \overline{AB} \\
1 & 1 & 1 & \overline{AB} (NAND) \\
\end{array} \]

\( V_2 \) and \( V_3 \) are used to increase the
turn-on threshold at the input
due to their forward voltage drop.

\(* Assume forward drop for diode is 0.7V. \)
Improvement to make TTL faster

- Totem pole output and transistor input replacing diodes (Eq. 7.32). Relation between $V_{dr}$, $V_{out}$ is the same.
- Give more drive current in the high state and faster response.

Start here

Lower impedance path in high state than BTL or DTL.

Changes through $Q_4$, $D$ and $100\Omega$ in high state.

Load capacitive.

Dual emitter transistor replaces diode logic in DTL

Note the parallel (to DTL)

$V_1$ or $V_2$ low $\Rightarrow$ ICQ1 > 0, $Q_2$ off $\Rightarrow$ output high
$V_1$ and $V_2$ high $\Rightarrow$ ICQ1 < 0, $Q_2$ on $\Rightarrow$ output low $Y = \bar{A} + \bar{B} = \bar{A} \bar{B}$ (see prob. handout)

Totem pole output stage

$Q_2$ controls $Q_0$ and $Q_3$

$Q_2$ off: $Q_4$ on, $Q_3$ off.

$\Rightarrow$ output high

$Q_2$ on:

$V_{CE_2} = 0.2$ (saturation)

$V_{B_3} = 0.8$ (saturation)

$V_{B_4} = V_{CE_2} = 1.0V$

$V_{out} = 0.2V$ ($V_{CE_2}$) (output)

The forward voltage drop across $D$ is big enough to keep $V_{BE_4} < 0.5V$ (off)

$V_{BE_4} + V_D = 1 - 0.2 = 0.8V$

$< \text{sum of cut-in voltage}$
Saturation may lead to long storage time, slowing BJT "off" transition (base region flooded with minority carriers, slowly diffuse out & be depletion region). Prevent saturation with Schottky diode.

- Metal-semiconductor junction - majority carrier device.
- Forward voltage drop 0.4 V rather than 0.7 V.
- Use to prevent BJT base-collector diode from being forward biased, prevent saturation.

\[
\begin{align*}
\text{Schottky Barrier} & \quad \text{N}^+ \quad \text{N} \\
\text{Al} & \quad \text{Lightly Doped} \\
\end{align*}
\]

\[
\begin{align*}
E_F & = E_F^s \\
E_F & = E_F^s \\
\text{Ref.: } & \text{G. Neudeck} \\
\text{PN Junction Diode} & \text{Addison Wesley}
\end{align*}
\]

For forward bias reduces the net field, raising the \( E_F \) level in the bulk, more electrons get over from semiconductor there is a depletion region, but there are no minority carriers.

For diode contact, use heavy doping, get tunneling through a narrow barrier (\( E_F \) within 3 kT of \( E_F^s \) for degenerate semiconductor)

SCHOTTKY TTL circuit - slightly different. See text.
TTL CIRCUIT MODIFICATIONS TO ALLOW USE WITH DATA BUS - OUTPUT INTERCONNECTION

OPEN COLLECTOR OUTPUT:

- **Rest on circuit**: open or closed switch to ground
- **High state**: (low state)

**Simplest case**:
- **Inverters**
- **Pull-up resistor**: e.g. 1kΩ

- **A switch**
- **Outputs "bussed"**
- **Open collector** (called "wired or" although logic may vary)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
<th>(with pull-up)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td></td>
</tr>
</tbody>
</table>

**Advantage**: Simple

**Disadvantage**: can be slow, depending on R value.

Two-input multiplier:

\[ Y = D_1 \cdot S + D_0 \cdot \bar{S} \]

- **Simplified logic table**
- **X = "don't care"**
- **Y = D_0**
- **Y = D_1**
Tri-state output:

3 possibilities: H, L, high impedance ("Z")

Better way to share I/O lines - active pull-up in high state, no external pull-up required.

TI circuit modification:

\[ \text{IF } OE \text{ is low, } Q_1 \text{ pulls the base of } Q_2 \text{ low, turning it off.} \\
\text{The } OE \text{ connection through the diode pulls the base of } Q_4 \text{ low, turning it off. Since } Q_2 \text{ is off,} \\
\text{the base of } Q_3 \text{ is at ground, so } Q_3 \text{ is off. Thus the} \\
\text{output is floating.} \Rightarrow \text{high impedance state.} \\
\text{If } OE \text{ is high, it has no further effect on circuit operation, as you can check.} \]

Two-input multiplexer:

\[ Y = D\overline{OE} + D1S \]

"0" indicates tri-state output.
n-MOS and p-MOS transistors as switches and CMOS inverter

(a) Enhancement mode MOSFET as inverter:

- **Threshold voltage** $V_T$
  
  - Approx. transfer characteristics:
    - FET below $V_T$ (off)
    - FET in ohmic region (on)

  So if we use logic levels with low $< V_T$ and high $\approx V_{DD}$, this is an inverter. Model MOSFET as an open switch with $V_{in} = $ low and closed switch (although with non-negligible resistance) with $V_{in} = $ high.

(b) By symmetry, p-MOS with source hooked to $+V_{DD}$ and drain through $R$ to ground would be open switch with $V_{in} = $ high, closed switch (with non-negligible $R$) with $V_{in} = $ low.

  The switch is closed to $+V_{DD}$ so output would be high with input low:

(c) CMOS inverter

- **CMOS inverter diagram**

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0$</td>
<td>$1$</td>
</tr>
<tr>
<td>$1$</td>
<td>$0$</td>
</tr>
</tbody>
</table>

Circuit structure - See text, Fig. 8.36

(See problem set for CMOS NAND example.)