Logic circuits & how they work

(1) Evolution from RTL inverter to DTL NAND to TTL NAND (and Schottky TTL).

BJT as switch - cutoff or saturation (discussed earlier)

For example (NOT TTL levels)
- $V_{in}$ low means $\approx 0.2\,V$
- $V_{in}$ high means $\geq 2\,V$

If $V_{in} \geq 2.0\,V$, $V_{BE} < 0.5\,V$,
BJT is cut off, $V_{out} \approx 5\,V$

If $V_{in} \geq 2\,V$, for reasonable $R$
transistor in saturation,
$V_{BE} \approx 0.8\,V$, $V_{out} \approx 0.2\,V$,
acting as logic inverter.

DTL NAND gate uses diodes to form logic (Fig. 7.26 in text)

If either $V_1$ or $V_2$
is at 0.2,
$V_3 = 0.9\,V$, not
enough to turn BJT on
(2 diode forward drops + 0.5
required)
(E.g., if $V_1 = 0.3$, $V_2 = 5\,V$,
$D_2$ is reverse biased,
but $D_3$ pulls BJT input
down.)

If both $V_1$ and $V_2$ are $+5$
current flows through $D_3$ to
pull $V_{BE}$ up to 0.8V
and output goes low.

$A \quad B \quad F$
---
0 0 1
0 1 1
1 0 1
1 1 0

$F = \overline{A\,B}$
(NAND)
Improvement to make TTL Pung

To form pole output and transistor input replacing diodes (Fig. 7.32). Relation between V_out, V_1, V_2 is the same.

Gives more drive current in the high state and faster response.

Start here

Lower impedance path in high state than DTL or RTL.

Changes through Q_4, D and 100k in high state.

Load capacitive

Totem pole output stage

Q_2 controls Q_1 and Q_3

Q_2 off: Q_4 on, Q_3 off.

⇒ output high

Q_2 on:

V_CE_2 = 0.2 (saturation)

V_B_3 = 0.8 (saturation)

V_B_4 = V_CE = 1.0V

V_out = 0.2V (V_CE) (output)

The forward voltage drop across D is big enough to keep V_B_4 < 0.5V (off)

V_B_4 + V_D = 1 - 0.2 = 0.8V

< sum of cut-in voltage

Diode of Q_1

Note the parallel (to DTL)

5k

Diode of Q_2

BJT provides current gain, an advantage over DTL.

Note unconventional "reverse active" mode when V_1 and V_2 are both high.

V_1 or V_2 low ⇒ IC_Q1 > 0, Q_2 off ⇒ output high

V_1 and V_2 high ⇒ IC_Q1 < 0, Q_2 on ⇒ output low ⇒ Y = \overline{A+B} = \overline{A}B

(see prob. handout)
Saturation may lead to long storage time, slowing BJT "off" transition (base region flooded with minority carriers, slowly diffuse out & be depletion region).
Present saturation with Schottky diode.
- Metal-semiconductor junction - majority carrier device.
- Forward voltage drop 0.4 V rather than 0.7V.
- Use to prevent BJT base-collector diode from being forward biased, prevent saturation.

![Schottky diode diagram]

Semiconductor
\[ v_{bbi} \]
\[ E_F \]
\[ E_v \]
\[ E_c \]

Change in levels in semiconductor
- From uncovered region
- Ions near boundary

Ref:
G. Neudeck
PN Junction Diode
Addison Wesley

BJT with Schottky diode clamp

Forward bias reduces the net field, raising the Ec level in the bulk, more electrons get over from semiconductor there is a depletion region, but there are no minority carriers.

For diode contact, use heavy doping, get tunneling through a narrow barrier (Es within 3kT of Ec for degenerate semiconductor)
TTL CIRCUIT MODIFICATIONS TO ALLOW USE WITH DATA BUS OUTPUT INTERCONNECTION

**Open Collector Output:**

- **Rest or Circuit:**
  
- **Open or Closed Switch to ground:**
  
- **Inverters:**
  
- **Pull-up resistor, e.g. 1 kΩ:**

**Simplest Case:**

- **A switch:**
  
- **Output "bussed" (called "wired or" although logic may vary):**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>( Y ) (with pull-up)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

**Advantage:** Simple

**Disadvantage:** Can be slow, depending on \( R \) value.

**Two-input Multiplexer:**

\[ Y = D_P \text{ if } S = 0 \]
\[ = D_1 \text{ if } S = 1 \]

\[ Y = D_P S + D_1 (\overline{S}) \]

**Simplified Logic Table:**

<table>
<thead>
<tr>
<th>S</th>
<th>D_I</th>
<th>D_P</th>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**X = "don't care"**
Tri-state output:

3 possibilities: H, L, high impedance ("Z")

- Better way to share bus lines - active pull-up in high state, no external pull-up required.

**TI circuit modification:**

\[ +5 \]

\[ 0 \]

\[ +5 \]

\[ Q_1 \]

\[ Q_2 \]

\[ Q_3 \]

A
B
OE

new emitter and base added

0 = low, 1 = high

<table>
<thead>
<tr>
<th>OE</th>
<th>A</th>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>High Impedance (&quot;Z&quot;)</td>
</tr>
</tbody>
</table>

**If OE is low, Q1 pulls the base of Q2 low, turning it off.**

The Q2 connection through the diode pulls the base of Q4 low, turning it off. Since Q2 is off, the base of Q3 is at ground, so Q3 is off. Thus the Y output is floating.

⇒ high impedance state.

If OE is high, it has no further effect on circuit operation, as you can check.

**Two-input multiplexer:**

\[ \text{Y} = D_1 \overline{D_0} \overline{S} + D_0 S \]

"S" indicates tri-state output.
n-Mos and p-Mos Transistors as Switches and CMOS Inverter

(a) Enhancement mode MOSFET as inverter:

\[ V_{in} \quad \text{See text, Fig. 8.23} \]

\[ V_{DD} \quad V_{DD} \]

Approx. transfer characteristics:

\[ \text{FET below } V_T \text{ (off)} \]

\[ \text{FET in ohmic region (on)} \]

\[ V_T \quad V_{in} \]

\[ V_{DD} \]

so if we use logic levels with Low \( < V_T \) and High \( \approx V_{DD} \), this is an inverter. Model MOSFET as open switch with \( V_{in} = \text{low} \) and closed switch (although with non-negligible resistance) with \( V_{in} = \text{high} \).

(b) By symmetry, p-Mos with source hooked to \( +V_{DD} \) and drain through \( R \) to ground would be open switch with \( V_{in} = \text{high} \), closed switch (with non-negligible \( R \)) with \( V_{in} = \text{low} \). The switch is closed to \( +V_{DD} \) so output would be high with input low:

\[ V_{out} = \overline{A} \quad \overline{A} \]

(c) CMOS Inverter

\[ V_{in} \quad \text{See text, Fig. 8.36} \]

\[ V_{out} = \overline{A} \quad \overline{A} \]

\[ A \quad \text{with active pull-up.} \]

\[ A \quad \text{n-Mos} \quad \text{p-Mos} \quad Y \]

\[ L \quad \text{off} \quad \text{on} \]

\[ H \quad \text{on} \quad \text{off} \]

(Very simple integrated circuit structure — See Text, Fig. 8.36)

→ See problem set for CMOS NAND example.