Figure 15.9
Two-input TTL NAND gate (active pull-up).

Example a
Problem →

Determine the status of each transistor and prepare a function table for the TTL circuit.

Q3, Q4 = p-channel  
Q1, Q2 = n-channel

Figure 15.8

Q2 - Q6 is an OR gate.

Figure 15.18
Two-input CMOS NAND gate.

Example 7
Problem →

Determine the status of each FET and prepare a function table for the CMOS circuit.