

Lab 12: Inside Digital ICs

U.C. Davis Physics 116B

INTRODUCTION

In this lab, we will "look inside" digital ICs and see how they work. To do this, we will construct simplified models of the circuits they contain.

1. RTL GATES

Construct the RTL inverter circuit shown in figure 1. Note that the input is an analog voltage from the potentiometer for now.

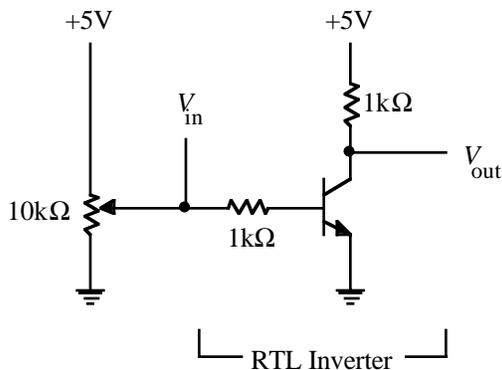


Figure 1: RTL inverter schematic.

For your lab report, make a graph of V_{out} vs. V_{in} . Use this graph to describe the function of an inverter. That is, what must a circuit do to invert a logic signal?

Now disconnect the potentiometer and connect the input of the inverter to a logic switch and the output to an LED monitor. Does it function as an inverter? (It should.)

Now drive the input with a square wave from the clock at the bottom of the logic station. (You can also use the function generator with a square wave with the voltages carefully set to +5V and 0V.) Look at the input and output on the oscilloscope. The output should be the inverse of the input with a small time delay as shown in figure 2.

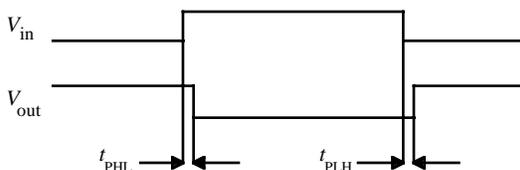


Figure 2: Propagation delay in the RTL inverter.

See if you can measure the propagation delays t_{PHL} (the time for the output to change from high to low) and t_{PLH} (low to high). Propagation delay is the main enemy of fast circuits; minimizing it is the goal of most device engineers. Which propagation delay is shorter? Can you guess why? For your lab report, make an oscilloscope sketch of V_{in} and V_{out} , give your measured t_{PHL} and t_{PLH} , and answer the questions.

Now modify your inverter to be a NOR gate with inputs A and B and output Q as shown in figure 3. Verify that this is indeed a NOR gate by experimentally constructing its truth table.

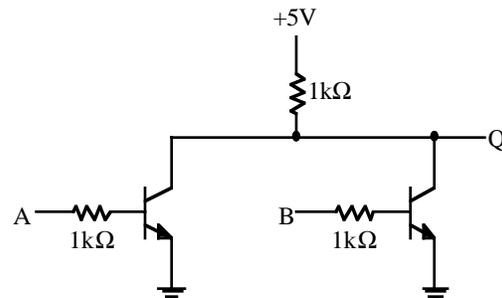


Figure 3: RTL NOR gate schematic.

To get the hang of this (and for your lab report), draw the RTL circuit for your favorite logic gate (which can't be NOR) and wire the circuit to verify that it works. You're now building logic gates!

2. STEP-BY-STEP D FLIP FLOP

You will now construct a D flip flop (a memory circuit) in several steps.

First, construct the S-R (set-reset) latch shown in figure 4. Determine the truth table for this circuit and explain why Q can be either 1 or 0 when A and B are both 1. Draw a timing diagram to illustrate how this circuit works as a memory device.

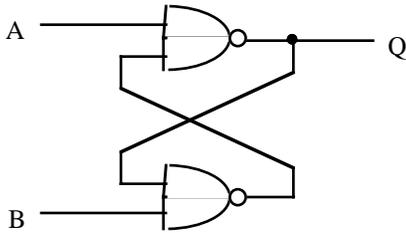


Figure 4: S-R latch.

Now modify the S-R latch to have a gated data input as shown in figure 5. This is the "transparent latch" circuit. Construct a truth table for this circuit and explain its operation using a timing diagram as you did for the S-R latch.

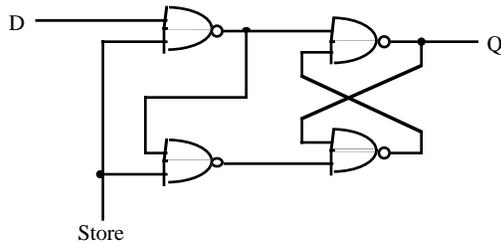


Figure 5: S-R latch with gated data input.

Now, add the rather crude edge trigger shown in figure 6 to your transparent latch. The complete circuit you now have should function like a D flip flop. Construct a truth table for this circuit and draw a timing diagram to illustrate how it works.

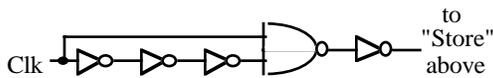


Figure 6: Edge trigger for D flip flop.

The entire D flip flop is usually represented by a box as used in figure 7. Use your D flip flop to construct the circuit shown in figure 7. This is a toggle circuit; each time the clock pulses, the output will toggle from 0 to 1 and then from 1 to 0. Draw a timing diagram to illustrate how this works.

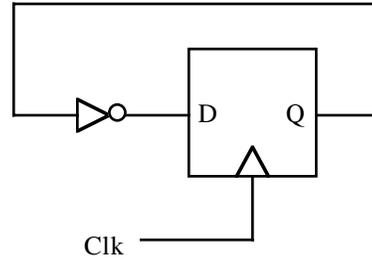


Figure 7: Toggle flip flop circuit.

Congratulations. You have now made all the basic building blocks you need to construct a computer or almost any other piece of digital equipment. In the next weeks, we will use already-built versions of these same circuits to construct ever more useful things.

3. OPEN-COLLECTOR OUTPUTS

IC's with "open collector outputs" still use the single transistor output of the RTL gate (without the pullup resistor). The outputs of these gates can be wired together to make a gate like the RTL NOR. This is called "wire-ORing". (*Never wire together the outputs of a normal IC!*) Construct the circuit of figure 8. For your lab report, give the complete truth table and logic diagram for this circuit. For the logic diagram, you will need to determine what type of gate the wire-ORed outputs act as. Note that this technique can be used to change voltage levels; the +5V can be replaced by +15V, for example.

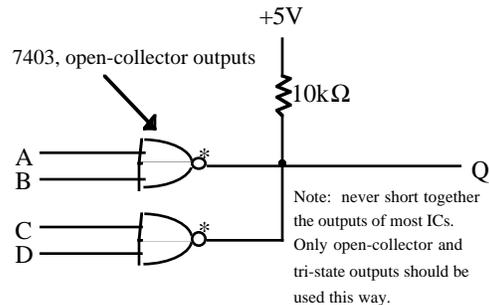


Figure 8: Wire-OR demonstration circuit.