Pulse problem 3 solution:

(a) \[ H(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \]

where \[ Z_1(s) = R_1 \frac{sC_1}{s^2R_1C_1 + 1} = \frac{R_1}{R_1 + \frac{1}{sC_1}} = \frac{R_1}{sR_1C_1 + 1} \]

\[ Z_2(s) = R_2 \frac{1}{sR_2C_2 + 1} \]

\[ H(s) = \frac{\frac{R_2}{sR_2C_2 + 1}}{\frac{R_2}{sR_2C_2 + 1} + \frac{R_2}{sR_2C_2 + 1}} = \frac{R_2}{10R_2} = \frac{1}{10} \]

(b) \[ Z(s) = Z_1(s) + Z_2(s) = \frac{9R_c}{20R_2C_2 + 1} + \frac{R_2}{sR_2C_2 + 1} = \frac{10R_c}{sR_2C_2 + 1} \]

\[ Z' = R_2 \frac{1}{sR'c' + 1} = \frac{10R_c}{s(10R_2)(0.1C_2) + 1} = \frac{10R_c}{sR_2C_2 + 1} \]

(c) \[ R_o = 1kR \]

For \( V_{\text{in}} \)

\[ R,T = \frac{0.35}{0.35} = 0.35 \times 2\pi R_c' \]

\[ R = R_o || R_l = 1kR || 1kR = 1kR \]

\[ = 0.35 \times 0.2\pi \times 1kR \times 5pF = 11 \text{ns} \]

and since \( H(s) \) is a constant (0.1), \( V_{\text{out}} \) must have the same form and rise time (assuming zero initial cond's).
11.51

\[ A \cdot B \cdot C \Rightarrow F = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C} + A \cdot B \cdot C \]

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\[ F = \overline{A} \cdot C + A \cdot B + B \cdot C \]

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TTL Circuit

\[
\begin{array}{c|c|c|c|c|c|c|c}
A & B & I_{CA1} & Q_1 & Q_2 & Q_3 & Q_4 & Y \\
\hline
0 & 0 & + & F & E & N & F & N \\
0 & 1 & + & F & F & N & F & N \\
1 & 0 & - & N & N & F & F & N \\
1 & 1 & - & N & N & F & F & F \\
\end{array}
\]

"AND"

\[\text{\(Q_1 \& Q_2\) are as in usual TTL NAND.}\]

A \(Q_8\) must both be high for \(I_{CA1}\) to be 1.

If \(I_{CA1}\) is 1, \(Q_2\) is "on", pulling base of \(Q_3\) to saturation (0.7 – 0.8V).

If \(Q_2\) is on, the base of \(Q_4\) is 0.2V so \(Q_4\) is off.

Thus, \(Q_6\) base is at ground and base of \(Q_5\) is pulled up.

The output 1.

In the other 3 cases \(I_{CA1}\) is 0, \(Q_2\) is off, \(Q_8\) is off, the base of \(Q_4\) is pulled up through the 2k\,\Omega\) resistor and diode. Since \(Q_4\) is off, the base of \(Q_6\) is pulled up and the voltage on the base of \(Q_5\) drops below the voltage necessary to turn it on. \(Q_4, Q_5, Q_6\) form the usual "totem pole" output stage of a TTL circuit.

CMOS Circuit: \(Q_1, Q_2, Q_3\) and \(Q_4\) perform the logic. \(Q_5\) and \(Q_6\) form an inverter.

\(Q_7\) and \(Q_8\) make another inverter. So the output is the same as the drain of \(Q_4\).

Switch representation of \(Q_1, Q_2, Q_3, Q_4\): 

\[V_{DD} \quad Q_1 \quad \overline{Q_2} \quad Y' \quad Q_3 \quad \overline{Q_4} \quad B \]

6 inverters

\[Q_3 \quad \overline{A} \quad Q_4 \quad B \]

Only "high" if \(A + B\) are both true.

\[Y' = \overline{AB} = A + B\]

Output is "NOR"

\[
\begin{array}{c|c|c|c|c|c|c|c}
A & B & Q_2 & Q_3 & Q_4 & Y' & Q_6 & Q_7 & Y \\
\hline
0 & 0 & N & N & F & F & F & N & F \\
0 & 1 & N & F & F & F & F & F & F \\
1 & 0 & F & F & N & F & N & F & F \\
1 & 1 & F & F & N & F & F & F & F \\
\end{array}
\]