**TTL Circuit**

\[
\begin{array}{c|cccc|c}
A & B & I_{CQ1} & Q_2 & Q_3 & Y \\
0 & 0 & 0 & F & F & N \\
0 & 1 & 0 & F & F & F \\
1 & 0 & 0 & F & F & F \\
1 & 1 & 0 & F & F & F \\
\end{array}
\]

Q1 & Q2 are as in usual TTL NAND.

A & B must both be high for I_{CQ1} to be "-":

**If I_{CQ1} is "-", Q2 is "on", pulling base of Q3 to saturation (0.7 V).**

**If Q2 is on", the base of Q3 is 0.2 V so Q3 is off.**

Thus, Q3 base is at ground and base of Q5 is pulled up.

The output "1." In the other 3 cases, I_{CQ1} is "+", Q2 is off, Q3 is off, the base of Q4 is pulled up through the 2kΩ resistor and diode. Since Q4 is on, the base of Q5 is pulled up and the voltage on the base of Q5 drops below the voltage necessary to turn it on. Q4, Q5 and Q6 form the usual "totem pole" output stage of a TTL circuit.

**CMOS Circuit:** Q1, Q2, Q3 and Q4 perform the logic, Q5 and Q6 form an inverter. Q7 and Q8 make another inverter. So the output is the same as the drain of Q4. Switch representation of Q1, Q2, Q3, Q4:

\[
\begin{align*}
V_{DD} & \quad \downarrow \\
Q_1 & \quad \bar{Y} \\
Q_2 & \quad Y \\
Q_3 & \quad \bar{A} \quad \bar{B} \\
Q_4 & \quad \bar{A} \quad \bar{B} \\
\end{align*}
\]

6 inverters

Only "high" if \( A \) & \( B \) are both false

\[ Y' = \overline{\overline{A \cdot B}} = A + B \]

Output is "NOR"