1. Switch model of circuit:

\[ 5V \]

\[ \overline{A} / M_1 \quad \overline{B} / M_2 \quad \overline{A} \] \[ \overline{B} / M_3 \quad M_4 \quad n-MOS \]

\[ \begin{array}{c|c|c|c|c|c}
A & B & \overline{A} & \overline{B} & A' & \overline{B}' & \text{Y} \\
\hline
F & F & 0 & 0 & \text{off} & \text{off} & H = T \\
F & T & 0 & 1 & \text{off} & \text{on} & L = F \\
T & F & 1 & 0 & \text{on} & \text{off} & L = F \\
T & T & 1 & 1 & \text{on} & \text{on} & L = F \\
\end{array} \]

\[ Y = A + B \text{ (nor)} \]

2. (a) The diodes are Schottky diodes (metal-semiconductor diodes).

(b) The diodes keep \( Q_1 \) and \( Q_2 \) in the active region when "on" rather than the saturation region. This is because they have a typical forward voltage drop of 0.4 V, less than the voltage \( V_B = 0.65 V \) for appreciable forward current to flow in the base-collector diode of the BJT. (Saturation results from both the BE and BC diodes being forward biased.) This reduces the minority carrier charge storage in the BJT base and allows the BJT circuit to turn off faster. The Schottky diode itself has negligible charge storage time since it has only majority carriers. Thus, the switching speed for the circuit is faster than standard TTL. See text and notes for details.
If A or B is low (or both), current flows from +5V through the 3.6 kΩ resistor to a diode anode and then to ground, so the forward biased Schottky anode is at ≈ 0.4V. Thus Q₁ is cut off (V_{BE} < 0.5V). Q₂ must also be cut off. The 1kΩ to +5V pulls Y to +5V (H).

If both A and B are high, both input diodes are reverse biased and the base of Q₂ is pulled up toward 5V through the 3.6 kΩ resistor. Q₁ will be "on" (in active region due to Schottky diode) and the base of Q₂ will be pulled up, turning it on as well. Thus Y is pulled low by Q₂. If V_{BE} of Q₂ (in active region) is 0.7V and V_{BC} = 0.4V due to the Schottky diode, V_{CE} = 0.3V (See Bobrow Table 7.3).

Truth table:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Q₁</th>
<th>Q₂</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>F</td>
<td>off</td>
<td>off</td>
<td>H = T</td>
</tr>
<tr>
<td>F</td>
<td>T</td>
<td>off</td>
<td>off</td>
<td>H = T</td>
</tr>
<tr>
<td>T</td>
<td>F</td>
<td>off</td>
<td>off</td>
<td>H = T</td>
</tr>
<tr>
<td>T</td>
<td>T</td>
<td>on</td>
<td>on</td>
<td>L = F</td>
</tr>
</tbody>
</table>

Y = \overline{AB} (NAND)
3. (a) \( CTEN = \text{low so counter always counts. } D/A \text{ high so counts down.} \)

\[
\text{Load} = Q_D Q_C Q_B Q_A \Rightarrow \{ \text{load with contents of inputs} \}
\]

\[
(12BA = 9) \text{ when counter reaches } 0100 = 4.
\]

**Complete state diagram:**

(b) \( 9 \rightarrow 8 \rightarrow 7 \rightarrow 6 \rightarrow 5 \rightarrow 9 \ldots \) (sequence just preceding clock pulse)

(c) State: \( 9 | 8 | 7 | 6 | 5 | 4 \)

\[
\text{"8" } Q_D
\]

\[
\text{"7" } Q_C
\]

\[
\text{"6" } Q_B
\]

\[
\text{"5" } Q_A
\]

Clock

\[
\text{Load} = Q_D Q_C Q_B Q_A
\]

\[
\text{possible } \text{glitch} \quad \text{possible } \text{glitch} \quad \text{Load} = "4"
\]

There are two possible glitches which could lead to premature transitions to state "9."
\[ F = A \cdot S + B \bar{S} \]

Glitch due to unequal gate delays

Both terms change at the same time when both A and B are high.

A \cdot S
B \bar{S}

\[ A \cdot S + B \bar{S} \]

Glitch without extra term.

\[ A \cdot S + B \bar{S} + A \bar{B} \]

(no glitch)

When both A and B are high, a glitch can occur since both terms (A \cdot S, B \bar{S}) change at the same time.

If either A or B (but not both) is low, only one term will change and the output will change accordingly when S changes, so no glitch.

If both A and B are low, both terms (A \cdot S, B \bar{S}) are low and don't change when S changes, so again no glitch. The extra term (A \cdot B) fixes the one possible glitch condition.
5V CMOS driving 3.3V CMOS:
The 5V CMOS can drive the 3.3V CMOS input at ≥5V. This is 1.7V above the supply voltage for the 3.3V device. I went to the Texas Instruments web site and downloaded the specifications for the 74HC1104 Hex inverter (advanced CMOS part). The allowed input voltage range is -0.5V to $V_{cc}+0.5V$ ($=3.8V$ for $V_{cc}=3.3V$). So $V_{in}=5V$ exceeds the allowable range. No good.

3.3V CMOS driving 5V CMOS:
Min H input level for 5V CMOS ≥ 3.4V.
Min H output level for 3.3V CMOS
is clearly ≤ 3.3V so can not drive 5V CMOS in the high state. Also no good.

* Upper limit on input is due to possibility of forward-biasing protective diodes on input lines leading to excessive current drawn from driving source. See Fig. 9.1 CMOS circuit in Horowitz and Hill, p. 567.
8 bit data lines D0-D7 go into magnitude comparator A inputs. 8 bit counter outputs go into A inputs. The clock frequency is 10 kHz x 2^8 = 2.56 MHz.

Method of operation: dA input is A.
Binary counter output is B.

Magnitude comparator A>B is the pulse-width modulated output.

The counter counts through all 256 states in the period of one 0.1 ms output cycle since the clock frequency is 256 x 10 kHz. Suppose D=10. The output will be high while 10 > Binary counter output (states 0-9), then it will be low until the counter returns to 0 (counting modulo 256). The larger D is, the longer the output stays on. If D=0, the output is always 0. If D=255, the output is on except for the last state.
Variations: one could use an "or" of "A=B" with "A>B" as output and get a short pulse for D=0 but with the output on continuously with D=255.