1. (a) \( D_b = \overline{D_a + D_b} \)

(b) flip-flop

(c) The circuit is synchronous because all transitions are synchronized with the clock pulse (i.e., clock inputs connect only to clock signals, not to other signals.)

(d) Minimum period = FF max. delay + FF max. delay + FF minimum setup time

\[ = 30\,\text{ns} + 15\,\text{ns} + 25\,\text{ns} = 70\,\text{ns} \]

(Not that constraint on min. clock pulse width of 20 ns can be easily satisfied with this period)

\[ f_{\text{max}} = \frac{1}{\text{min. period}} = 14.3\,\text{MHz}. \]
2. (a) The counter is initially 0. It counts up until \( Q_1 \) and \( Q_2 \) are both 1, at which point the count enable (active low) input goes to 1 and further counting is disabled. Thus, the counter is in the state \( 0110 = \text{"6"} \) and the output is \( 1 \cdot 1 = 0 \).

(b) The counter is reset to zero, so count enable = 0 and remains 0 at the clock transitions until the state "6" is reached. During this time the output is high. The minimum length of the output pulse is slightly more than 5 clock cycles (the clear input must arrive slightly before the clock transition for an immediate 0 → 1 transition of the counter. Then there are 5 fall states (1, 2, 3, 4, 5). On the sixth clock edge, the reaches 6, the output goes low and counting stops.

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Output: _
Input: _
Clock: ___________
Counter State: 6→1→0→2→3→4→5→6...
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Min. output pulse width = 5 x 10 ns = 50 ns

(c) The output pulse is extended to \( \geq 50 \) ns after the second pulse (second input resets the counter to 0).

(d) Yes—For example, in the transition from 011 to 100, the 110 state can momentarily appear and result in a glitch (toward 0) of the output pulse. (This will not affect the count sequence since the glitch is momentary and does not come during the "setup time" for the clock enable input. A glitch on the clear input is another story).