HI5812

CMOS 20 Microsecond, 12-Bit, Sampling A/D Converter with Internal Track and Hold

Features

- Conversion Time ...................... 20µs
- Throughput Rate ...................... 50 KSPS
- Built-In Track and Hold
- Guaranteed No Missing Codes Over Temperature
- Single Supply Voltage .................. +5V
- Maximum Power Consumption .......... 25mW
- Internal or External Clock

Applications

- Remote Low Power Data Acquisition Systems
- Digital Audio
- DSP Modems
- General Purpose DSP Front End
- µP Controlled Measurement System
- Professional Audio Positioner/Fader

Description

The HI5812 is a fast, low power, 12-bit, successive approximation analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws just 1.9mA when operating at 5V. The HI5812 features a built-in track and hold. The conversion time is as low as 15µs with a 5V supply.

The twelve data outputs feature full high speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. The output is user selectable: (i.e.) 12-bit, 8-bit (MSBs), and/or 4-bit (LSBs). A data ready flag, and conversion-start inputs complete the digital interface.

An internal clock is provided and is available as an output. The clock may also be over-driven by an external source.

Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>INL (LSB) (MAX OVER TEMP.)</th>
<th>TEMP. RANGE (ºC)</th>
<th>PACKAGE</th>
<th>PKG. NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>HI5812JIP</td>
<td>±1.5</td>
<td>-40 to 85</td>
<td>24 Ld PDIP</td>
<td>E24.3</td>
</tr>
<tr>
<td>HI5812KIP</td>
<td>±1.0</td>
<td>-40 to 85</td>
<td>24 Ld PDIP</td>
<td>E24.3</td>
</tr>
<tr>
<td>HI5812JIB</td>
<td>±1.5</td>
<td>-40 to 85</td>
<td>24 Ld SOIC</td>
<td>M24.3</td>
</tr>
<tr>
<td>HI5812KIB</td>
<td>±1.0</td>
<td>-40 to 85</td>
<td>24 Ld SOIC</td>
<td>M24.3</td>
</tr>
<tr>
<td>HI5812JJU</td>
<td>±1.5</td>
<td>-40 to 85</td>
<td>24 Ld CERDIP</td>
<td>F24.3</td>
</tr>
<tr>
<td>HI5812KIU</td>
<td>±1.0</td>
<td>-40 to 85</td>
<td>24 Ld CERDIP</td>
<td>F24.3</td>
</tr>
</tbody>
</table>

Pinout

![HI5812 Pinout Diagram](image-url)
Functional Block Diagram

TO INTERNAL LOGIC

V_DD  V_SS  V_IN

V_REF+  V_REF-

V_AA+  V_AA-

50Ω SUBSTRATE

12-BIT SUCCESSIVE APPROXIMATION REGISTER

12-BIT EDGE TRIGGERED "D" LATCHED

CONTROL & TIMING

CLOCK

DRDY

CLK

OEM

D11 (MSB)

D10

D9

D8

D7

D6

D5

D4

D3

D2

D1

D0 (LSB)

OEL

STRT
Absolute Maximum Ratings

Supply Voltage
- $V_{DD}$ to $V_{SS}$: $(V_{SS} - 0.5V) < V_{DD} < +6.5V$
- $V_{AA+}$ to $V_{AA-}$: $(V_{SS} - 0.5V)$ to $(V_{SS} + 6.5V)$
- $V_{AA+}$ to $V_{DD}$: $\pm 0.3V$

Analog and Reference Inputs
- $V_{IN}$, $V_{REF+}$, $V_{REF-}$: $(V_{SS} - 0.3V) < V_{IN} < (V_{DD} + 0.3V)$

Digital I/O Pins
- $(V_{SS} - 0.3V) < V_{I/O} < (V_{DD} + 0.3V)$

Operating Conditions

Temperature Range
- PDIP, SOIC, and CERDIP Packages: $-40^\circ C$ to $85^\circ C$

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

Thermal Information

<table>
<thead>
<tr>
<th>Package</th>
<th>$\theta_{JA}$ (°C/W)</th>
<th>$\theta_{JC}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CERDIP</td>
<td>60</td>
<td>12</td>
</tr>
<tr>
<td>PDIP</td>
<td>80</td>
<td>N/A</td>
</tr>
<tr>
<td>SOIC</td>
<td>75</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Maximum Junction Temperature
- Plastic Packages: $150^\circ C$
- Ceramic Package: $175^\circ C$
- Maximum Storage Temperature Range: $-65^\circ C$ to $150^\circ C$
- Maximum Lead Temperature (Soldering, 10s): $300^\circ C$

Electrical Specifications

$V_{DD} = V_{AA+} = 5V$, $V_{REF+} = +4.608V$, $V_{SS} = V_{AA-} = V_{REF-} = GND$, $CLK = \text{External 750kHz}$, Unless Otherwise Specified

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>25°C</th>
<th>-40°C TO 85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>Resolution</td>
<td></td>
<td>12</td>
<td>-</td>
</tr>
<tr>
<td>Integral Linearity Error, INL</td>
<td>J</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(End Point)</td>
<td>K</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Differential Linearity Error, DNL</td>
<td>J</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(Adjustable to Zero)</td>
<td>K</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Gain Error, FSE</td>
<td>J</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(Adjustable to Zero)</td>
<td>K</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Offset Error, $V_{OS}$</td>
<td>J</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>(Adjustable to Zero)</td>
<td>K</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Power Supply Rejection, PSRR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Error PSRR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain Error PSRR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{REF} = 4V$</td>
<td></td>
<td>0.1</td>
<td>±0.5</td>
</tr>
<tr>
<td>$V_{DD} = V_{AA+} = 5V \pm 5%$</td>
<td></td>
<td>0.1</td>
<td>±0.5</td>
</tr>
</tbody>
</table>

DYNAMIC CHARACTERISTICS

Signal to Noise Ratio, SINAD
- RMS Signal
  - $f_S = \text{Internal Clock}$, $f_{IN} = 1kHz$
  - $f_S = 750kHz$, $f_{IN} = 1kHz$
- $-68.8$ dB to $-69.2$ dB

RMS Noise + Distortion
- $f_S = \text{Internal Clock}$, $f_{IN} = 1kHz$
- $f_S = 750kHz$, $f_{IN} = 1kHz$
- $71.0$ dB to $71.5$ dB

Signal to Noise Ratio, SNR
- RMS Signal
  - $f_S = \text{Internal Clock}$, $f_{IN} = 1kHz$
  - $f_S = 750kHz$, $f_{IN} = 1kHz$
- $-70.5$ dB to $-71.1$ dB

RMS Noise
- $f_S = \text{Internal Clock}$, $f_{IN} = 1kHz$
- $f_S = 750kHz$, $f_{IN} = 1kHz$
- $71.5$ dB to $72.1$ dB

Total Harmonic Distortion, THD
- $f_S = \text{Internal Clock}$, $f_{IN} = 1kHz$
- $f_S = 750kHz$, $f_{IN} = 1kHz$
- $-73.9$ dB to $-73.8$ dB

Spurious Free Dynamic Range, SFDR
- $f_S = \text{Internal Clock}$, $f_{IN} = 1kHz$
- $f_S = 750kHz$, $f_{IN} = 1kHz$
- $-75.4$ dB to $-75.1$ dB

- $6-1791$
## Electrical Specifications

\[ V_{DD} = V_{AA}^+ = 5V, V_{REF^+} = +4.608V, V_{SS} = V_{AA}^- = V_{REF^-} = GND, \text{CLK} = \text{External 750kHz}, \text{Unless Otherwise Specified} \]

### ANANLIG INPUT

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>25°C</th>
<th>-40°C TO 85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>Input Current, Dynamic</td>
<td>At ( V_{IN} = V_{REF^+}, 0V )</td>
<td>-</td>
<td>±50</td>
</tr>
<tr>
<td>Input Current, Static</td>
<td>Conversion Stopped</td>
<td>-</td>
<td>±0.4</td>
</tr>
<tr>
<td>Input Bandwidth -3dB</td>
<td></td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>Reference Input Current</td>
<td></td>
<td>-</td>
<td>160</td>
</tr>
<tr>
<td>Input Series Resistance, ( R_S )</td>
<td>In Series with Input ( C_{SAMPLE} )</td>
<td>-</td>
<td>420</td>
</tr>
<tr>
<td>Input Capacitance, ( C_{SAMPLE} ) During Sample State</td>
<td>-</td>
<td>380</td>
<td>-</td>
</tr>
<tr>
<td>Input Capacitance, ( C_{HOLD} ) During Hold State</td>
<td>-</td>
<td>20</td>
<td>-</td>
</tr>
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### DIGITAL INPUTS OEL, OEM, STRT

<table>
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<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>25°C</th>
<th>-40°C TO 85°C</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>High-Level Input Voltage, ( V_{IH} )</td>
<td></td>
<td>2.4</td>
<td>-</td>
</tr>
<tr>
<td>Low-Level Input Voltage, ( V_{IL} )</td>
<td></td>
<td>-</td>
<td>- 0.8</td>
</tr>
<tr>
<td>Input Leakage Current, ( I_{IL} ) Except CLK, ( V_{IN} = 0V, 5V )</td>
<td>-</td>
<td>-</td>
<td>±10</td>
</tr>
<tr>
<td>Input Capacitance, ( C_{IN} )</td>
<td></td>
<td>- 10</td>
<td>-</td>
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### DIGITAL OUTPUTS

<table>
<thead>
<tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
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<tr>
<td>High-Level Output Voltage, ( V_{OH} ) ISOURCE = -400( \mu A )</td>
<td></td>
<td>4.6</td>
<td>-</td>
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<tr>
<td>Low-Level Output Voltage, ( V_{OL} ) ISINK = 1.6( mA )</td>
<td></td>
<td>-</td>
<td>- 0.4</td>
</tr>
<tr>
<td>Three-State Leakage, ( I_{OZ} ) Except DRDY, ( V_{OUT} = 0V, 5V )</td>
<td>-</td>
<td>-</td>
<td>±10</td>
</tr>
<tr>
<td>Output Capacitance, ( C_{OUT} ) Except DRDY</td>
<td>-</td>
<td>20</td>
<td>-</td>
</tr>
</tbody>
</table>

### CLOCK

<table>
<thead>
<tr>
<th>Parameter</th>
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<th>25°C</th>
<th>-40°C TO 85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>High-Level Output Voltage, ( V_{OH} ) ISOURCE = -100( \mu A ) (Note 2)</td>
<td></td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>Low-Level Output Voltage, ( V_{OL} ) ISINK = 100( \mu A ) (Note 2)</td>
<td></td>
<td>-</td>
<td>- 1</td>
</tr>
<tr>
<td>Input Current CLK Only, ( V_{IN} = 0V, 5V )</td>
<td></td>
<td>-</td>
<td>- ±5</td>
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</table>

### TIMING

<table>
<thead>
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<th>Parameter</th>
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<th>-40°C TO 85°C</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>Conversion Time ( t_{CONV} + t_{ACQ} ) (Includes Acquisition Time)</td>
<td></td>
<td>20</td>
<td>-</td>
</tr>
<tr>
<td>Clock Frequency Internal Clock, (CLK = Open)</td>
<td></td>
<td>200</td>
<td>300</td>
</tr>
<tr>
<td>External CLK (Note 2)</td>
<td></td>
<td>0.05</td>
<td>2</td>
</tr>
<tr>
<td>Clock Pulse Width, ( t_{LOW}, t_{HIGH} ) External CLK (Note 2)</td>
<td></td>
<td>100</td>
<td>-</td>
</tr>
<tr>
<td>Aperture Delay, ( t_{APR} ) (Note 2)</td>
<td></td>
<td>-</td>
<td>35</td>
</tr>
<tr>
<td>Clock to Data Ready Delay, ( t_{D_{R_DRDY}} ) (Note 2)</td>
<td></td>
<td>-</td>
<td>105</td>
</tr>
<tr>
<td>Clock to Data Ready Delay, ( t_{D_{D_DRDY}} ) (Note 2)</td>
<td></td>
<td>-</td>
<td>100</td>
</tr>
<tr>
<td>Start Removal Time, ( t_{STRY} ) (Note 2)</td>
<td></td>
<td>75</td>
<td>30</td>
</tr>
<tr>
<td>Start Setup Time, ( t_{SU_DRDY} ) (Note 2)</td>
<td></td>
<td>85</td>
<td>60</td>
</tr>
<tr>
<td>Start Pulse Width, ( t_{SW_{DRDY}} ) (Note 2)</td>
<td></td>
<td>10</td>
<td>4</td>
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<tr>
<td>Start to Data Ready Delay, ( t_{D_{D_DRDY}} ) (Note 2)</td>
<td></td>
<td>-</td>
<td>65</td>
</tr>
<tr>
<td>Clock Delay from Start, ( t_{S_DRDY} ) (Note 2)</td>
<td></td>
<td>-</td>
<td>60</td>
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<tr>
<td>Output Enable Delay, ( t_{EN} ) (Note 2)</td>
<td></td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>Output Disabled Delay, ( t_{DIS} ) (Note 2)</td>
<td></td>
<td>-</td>
<td>80</td>
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### POWER SUPPLY CHARACTERISTICS

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<th>Parameter</th>
<th>Test Conditions</th>
<th>25°C</th>
<th>-40°C TO 85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>Supply Current, ( I_{DD} + I_{AA} )</td>
<td></td>
<td>- 1.9</td>
<td>5</td>
</tr>
</tbody>
</table>

**NOTE:**

2. Parameter guaranteed by design or characterization, not production tested.
**Timing Diagrams**

**FIGURE 1. CONTINUOUS CONVERSION MODE**

- **CLK (EXTERNAL OR INTERNAL)**
- **START**
- **DRDY**
- **D0 - D11**
- **V_IN**
- **OEL = OEN = V_SS**

**FIGURE 2. SINGLE SHOT MODE EXTERNAL CLOCK**

- **CLK (EXTERNAL)**
- **START**
- **DRDY**
- **V_IN**
Timing Diagrams (Continued)

FIGURE 3. SINGLE SHOT MODE INTERNAL CLOCK

FIGURE 4A. FIGURE 4B.

FIGURE 4. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

FIGURE 5. GENERAL TIMING LOAD CIRCUIT
Typical Performance Curves

**FIGURE 6. INL vs TEMPERATURE**

**FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE**

**FIGURE 8. DNL vs TEMPERATURE**

**FIGURE 9. ACCURACY vs REFERENCE VOLTAGE**

**FIGURE 10. FULL SCALE ERROR vs TEMPERATURE**

**FIGURE 11. POWER SUPPLY REJECTION vs TEMPERATURE**

- $V_{DD} = V_{AA+} = 5V, V_{REF+} = 4.608V$
- $V_{DD} = V_{AA+} = 5V, V_{REF+} = 4.608V$
- $V_{DD} = V_{AA+} = 5V, V_{REF+} = 4.608V$
Typical Performance Curves (Continued)

**FIGURE 12. SUPPLY CURRENT vs TEMPERATURE**

- **V_DD = V_AA+ = 5V, V_REF+ = 4.608V**
- SUPPLY CURRENT, I_DD (mA)
- TEMPERATURE (°C)

**FIGURE 13. FFT SPECTRUM**

- INPUT FREQUENCY = 1kHz
- SAMPLING RATE = 50kHz
- SNR = 72.1dB
- SINAD = 71.4dB
- EFFECTIVE BITS = 11.5
- THD = -79.1dBc
- PEAK NOISE = -80.9dB
- SFDR = -80.9dB
- SNR = 71.4dB
- INPUT FREQUENCY (kHz)
- AMPLITUDE (dB)
- FREQUENCY BINS

**FIGURE 14. INTERNAL CLOCK FREQUENCY vs TEMPERATURE**

- **V_DD = V_AA+ = 5V, V_REF+ = 4.608V**
- INTERNAL CLOCK FREQUENCY (kHz)
- TEMPERATURE (°C)

**FIGURE 15. EFFECTIVE BITS vs INPUT FREQUENCY**

- **V_DD = V_AA+ = 5V, V_REF+ = 4.608V**
- INTERNAL CLOCK FREQUENCY (kHz)
- EFFECTIVE BITS
- INPUT FREQUENCY (kHz)
- A. CLK = INTERNAL
- B. CLK = 750kHz
- C. CLK = 1MHz

**FIGURE 16. TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY**

- **V_DD = V_AA+ = 5V, V_REF+ = 4.608V**
- INTERNAL CLOCK FREQUENCY (kHz)
- THD (dBc)
- INPUT FREQUENCY (kHz)
- A. CLK = INTERNAL
- B. CLK = 750kHz
- C. CLK = 1MHz

**FIGURE 17. SIGNAL NOISE RATIO vs INPUT FREQUENCY**

- **V_DD = V_AA+ = 5V, V_REF+ = 4.608V**
- INTERNAL CLOCK FREQUENCY (kHz)
- SNR (dBc)
- INPUT FREQUENCY (kHz)
- A. CLK = INTERNAL
- B. CLK = 750kHz
- C. CLK = 1MHz
Theory of Operation

HI5812 is a CMOS 12-Bit Analog-to-Digital Converter that uses capacitor-charge balancing to successively approximate the analog input. A binarily weighted capacitor network forms the A/D heart of the device. See the block diagram for the HI5812.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, $V_{REF+}$ or $V_{REF-}$.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto-balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the $V_{REF+}$ terminal; and the remaining capacitors to $V_{REF-}$. The capacitor-common node, after the charges balance out, will indicate whether the input was above $1/2$ of $(V_{REF+} - V_{REF-})$. At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to $V_{REF+}$ (if the comparator was high) or returned to $V_{REF-}$. This allows the next comparison to be at either $3/4$ or $1/4$ of $(V_{REF+} - V_{REF-})$.

At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at $V_{REF+}$ or at $V_{REF-}$.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data-ready output goes active. The conversion cycle is now complete.

Analog Input

The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than $5\mu$A and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period as shown in Figure 18. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DRDY</td>
<td>Output flag signifying new data is available. Goes high at end of clock period 15. Goes low when new conversion is started.</td>
</tr>
<tr>
<td>2</td>
<td>D0</td>
<td>Bit 0 (Least Significant Bit, LSB).</td>
</tr>
<tr>
<td>3</td>
<td>D1</td>
<td>Bit 1.</td>
</tr>
<tr>
<td>4</td>
<td>D2</td>
<td>Bit 2.</td>
</tr>
<tr>
<td>5</td>
<td>D3</td>
<td>Bit 3.</td>
</tr>
<tr>
<td>6</td>
<td>D4</td>
<td>Bit 4.</td>
</tr>
<tr>
<td>7</td>
<td>D5</td>
<td>Bit 5.</td>
</tr>
<tr>
<td>8</td>
<td>D6</td>
<td>Bit 6.</td>
</tr>
<tr>
<td>9</td>
<td>D7</td>
<td>Bit 7.</td>
</tr>
<tr>
<td>10</td>
<td>D8</td>
<td>Bit 8.</td>
</tr>
<tr>
<td>11</td>
<td>D9</td>
<td>Bit 9.</td>
</tr>
<tr>
<td>12</td>
<td>$V_{SS}$</td>
<td>Digital Ground (0V).</td>
</tr>
<tr>
<td>13</td>
<td>D10</td>
<td>Bit 10.</td>
</tr>
<tr>
<td>14</td>
<td>D11</td>
<td>Bit 11 (Most Significant Bit, MSB).</td>
</tr>
<tr>
<td>15</td>
<td>OEM</td>
<td>Three-State Enable for D4-D11. Active low input.</td>
</tr>
<tr>
<td>16</td>
<td>$V_{AA-}$</td>
<td>Analog Ground. (0V).</td>
</tr>
<tr>
<td>17</td>
<td>$V_{AA+}$</td>
<td>Analog Positive Supply. (+5V) (See text.)</td>
</tr>
<tr>
<td>18</td>
<td>$V_{IN}$</td>
<td>Analog Input.</td>
</tr>
<tr>
<td>19</td>
<td>$V_{REF+}$</td>
<td>Reference Voltage Positive Input, sets 4095 code end of input range.</td>
</tr>
<tr>
<td>20</td>
<td>$V_{REF-}$</td>
<td>Reference Voltage Negative Input, sets 0 code end of input range.</td>
</tr>
<tr>
<td>21</td>
<td>STRT</td>
<td>Start Conversion Input Active Low, recognized after end of clock period 15.</td>
</tr>
<tr>
<td>22</td>
<td>CLK</td>
<td>CLK Input or Output. Conversion functions are synchronized to positive going edge. (See text.)</td>
</tr>
<tr>
<td>23</td>
<td>OEL</td>
<td>Three-State Enable for D0 D3. Active Low Input.</td>
</tr>
<tr>
<td>24</td>
<td>$V_{DD}$</td>
<td>Digital Positive Supply (+5V).</td>
</tr>
</tbody>
</table>

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the $V_{REF+}$ terminal; and the remaining capacitors to $V_{REF-}$. The capacitor-common node, after the charges balance out, will indicate whether the input was above $1/2$ of $(V_{REF+} - V_{REF-})$. At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to $V_{REF+}$ (if the comparator was high) or returned to $V_{REF-}$. This allows the next comparison to be at either $3/4$ or $1/4$ of $(V_{REF+} - V_{REF-})$.

At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at $V_{REF+}$ or at $V_{REF-}$.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data-ready output goes active. The conversion cycle is now complete.

Analog Input

The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than $5\mu$A and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period as shown in Figure 18. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.

![Figure 18. Typical Analog Input Current](image)
As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 clock cycles. With an external clock of 750kHz the track period is 4µs.

A simplified analog input model is presented in Figure 19. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external “zero Ω” source to 0.5 LSB (1/8192), the charging time must be at least 9 time constants or 1.4µs. The maximum source impedance (R_{SOURCE(Max)}) for a 4µs acquisition time settling to within 0.5LSB is 750Ω.

If the clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.

![Figure 19. Analog Input Model in Track Mode](image)

**Reference Input**

The reference input V_{REF+} should be driven from a low impedance source and be well decoupled.

As shown in Figure 20, current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge-balancing capacitors are switched between V_{REF-} and V_{REF+} (clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore V_{REF+} and V_{REF-} should be well bypassed. Reference input V_{REF+} is normally connected directly to the analog ground plane. If V_{REF-} is biased for nulling the converters offset it must be stable during the conversion cycle.

The HI5812 is specified with a 4.608V reference, however, it will operate with a reference down to 3V having a slight degradation in performance. A typical graph of accuracy vs reference voltage is presented.

**Full Scale and Offset Adjustment**

In many applications the accuracy of the HI5812 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The V_{REF+} and V_{REF-} pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the V_{REF-} might be returned to a clean ground, and the offset adjustment done on an input amplifier. V_{REF+} would then be adjusted to null out the full scale error. When this is not possible, the V_{REF-} input can be adjusted to null the offset error, however, V_{REF+} must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).

**Control Signal**

The HI5812 may be synchronized from an external source by using the STRT (Start Conversion) input to initiate conversion, or if STRT is tied low, may be allowed to free run. Each conversion cycle takes 15 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by t_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by t_D1DRDY) after the start of clock period 1, and returns low (specified by t_D2DRDY) after the start of clock period 2.

The 12 data bits are available in parallel on three-state bus driver outputs. When low, the OEM input enables the most significant byte (D4 through D11) while the OEL input enables the four least significant bits (D0 - D3). t_EN and t_DIS specify the output enable and disable times.

If the output data is to be latched externally, either the trailing edge of data ready or the next falling edge of the clock after data ready goes high can be used.

When STRT input is used to initiate conversions, operation is slightly different depending on whether an internal or external clock is used.

Figure 3 illustrates operation with an internal clock. If the STRT signal is removed (at least t_D2STRT) before clock period 1, and is not reapplied during that period, the clock will shut off after entering period 2. The input will continue to track and the DRDY output will remain high during this time.

A low signal applied to STRT (at least t_D2STRT wide) can now initiate a new conversion. The STRT signal (after a delay of t_D2STRT) causes the clock to restart.

Depending on how long the clock was shut off, the low portion of clock period 2 may be longer than during the remaining cycles.
The input will continue to track until the end of period 3, the same as when free running.

Figure 2 illustrates the same operation as above but with an external clock. If STRT is removed (at least tRSTR) before clock period 2, a low signal applied to STRT will drop the DRDY flag as before, and with the first positive-going clock edge that meets the (tUSTR) setup time, the converter will continue with clock period 3.

Clock

The HI5812 can operate either from its internal clock or from one externally supplied. The CLK pin functions either as the clock output or input. All converter functions are synchronized with the rising edge of the clock signal.

Figure 21 shows the configuration of the internal clock. The clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and stray wiring capacitance should be kept to a minimum.

The internal clock will shut down if the A/D is not restarted after a conversion. The clock could also be shut down with an open collector driver applied to the CLK pin. This should only be done during the sample portion (the first three clock periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold.

If an external clock is supplied to the CLK pin, it must have sufficient drive to overcome the internal clock source. The external clock can be shut off, but again, only during the sample portion of a conversion cycle. At other times, it must be above the minimum frequency shown in the specifications.

In the above two cases, a further restriction applies in that the clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge-pump voltage to decay.

If the internal or external clock was shut off during the conversion time (clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

An external clock must also meet the minimum tLOW and tHIGH times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

Power Supplies and Grounding

VDD and VSS are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the VDD and VSS lines, VSS should have a low impedance path to digital ground and VDD should be well bypassed.

Except for VAA+, which is a substrate connection to VDD, all pins have protection diodes connected to VDD and VSS. Input transients above VDD or below VSS will get steered to the digital supplies.

The VAA+ and VAA- terminals supply the charge-balancing comparator only. Because the comparator is autobalanced between conversions, it has good low-frequency supply rejection. It does not reject well at high frequencies however; VAA should be returned to a clean analog ground and VAA+ should be RC decoupled from the digital supply as shown in Figure 22.

There is approximately 50Ω of substrate impedance between VDD and VAA+. This can be used, for example, as part of a low-pass RC filter to attenuate switching supply noise. A 10µF capacitor from VAA+ to ground would attenuate 30kHz noise by approximately 40dB. Note that back-to-back diodes should be placed from VDD to VAA+ to handle supply to capacitor turn-on or turn-off current spikes.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the A/D. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured RMS signal to RMS sum of noise at a specified input and sampling frequency. The noise is the RMS sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76) dB. For an ideal 12-bit converter the SNR is 74dB. Differential and integral linearity errors will degrade SNR.

\[
SNR = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}
\]

Signal-To-Noise + Distortion Ratio

SINAD is the measured RMS signal to RMS sum of noise plus harmonic power and is expressed by the following:

\[
SINAD = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd - 6th)}}
\]

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data:

\[
ENOB = \frac{\text{SINAD} - 1.76}{6.02}
\]
Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

\[
THD = 10 \log \left( \frac{\text{Total Harmonic Power (2nd - 6th Harmonic)}}{\text{Sinewave Signal Power}} \right)
\]

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

\[
SFDR = 10 \log \left( \frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}} \right)
\]

<table>
<thead>
<tr>
<th>CODE DESCRIPTION</th>
<th>INPUT VOLTAGE†</th>
<th>DECIMAL COUNT</th>
<th>BINARY OUTPUT CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VREF+ = 4.608V VREF- = 0.0V (V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full Scale (FS)</td>
<td>4.6069</td>
<td>4095</td>
<td>D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0</td>
</tr>
<tr>
<td></td>
<td>4.6058</td>
<td>4094</td>
<td>1 1 1 1 1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>3/4 FS</td>
<td>3.4560</td>
<td>3072</td>
<td>1 1 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1/2 FS</td>
<td>2.3040</td>
<td>2048</td>
<td>1 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1/4 FS</td>
<td>1.1520</td>
<td>1024</td>
<td>0 1 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1 LSB</td>
<td>0.001125</td>
<td>1</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>Zero</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
</tbody>
</table>

† The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

FIGURE 22. GROUND AND SUPPLY DECOUPLING
Die Characteristics

DIE DIMENSIONS:
3200µm x 3940µm

METALLIZATION:
Type: AlSi
Thickness: 11kÅ ±1kÅ

PASSIVATION:
Type: PSG
Thickness: 13kÅ ±2.5kÅ

WORST CASE CURRENT DENSITY:
1.84 x 10^5 A/cm²

Metallization Mask Layout