Synchronous Sequential Circuit Design

**Example:** synchronous ÷3 counter with "count enable" input and "carry" output.
Use Mealy model: output depends on state & input. The transition diagram is given in the next section.

![Transition Diagram]

**State assignment (make self-starting):**

We wish to implement the following transition diagram using JK flip-flops and gates:

![Transition Diagram]

Each state will be represented by two flip-flops, A and B:

\[
\begin{align*}
J_A &\quad Q_A &\quad T_A &\quad Q_B \\
K_A &\quad K_A &\quad T_B &\quad Q_B
\end{align*}
\]

Thus, the state 10 is represented by \( Q_A = 1, Q_B = 0 \).
Let \( D \) represent the input signal and \( E \) the output.
We now need to figure out how to write functions for $J_A$, $K_A$, $J_B$, $K_B$, and $E$ as functions of $Q_A$, $Q_B$, and $D$.

Step I: make a transition map for each flip-flop which tells what the flip-flop is supposed to do at each transition of the diagram above. The transition map is a Karnaugh map with elements as shown in the table below:

<table>
<thead>
<tr>
<th>Flip-flop transition</th>
<th>Element in transition K. map</th>
</tr>
</thead>
<tbody>
<tr>
<td>$1 \rightarrow 1$</td>
<td>$1$</td>
</tr>
<tr>
<td>$0 \rightarrow 0$</td>
<td>$0$</td>
</tr>
<tr>
<td>$0 \rightarrow 1$</td>
<td>$d$</td>
</tr>
<tr>
<td>$1 \rightarrow 0$</td>
<td>$\beta$</td>
</tr>
<tr>
<td>don't care</td>
<td>$x$</td>
</tr>
</tbody>
</table>

For example, the transition map for flip-flop A is:

```
A: 0 | 0 | 0 | 0 | 1 | 1 |
   0 | 0 | 0 | 0 | 1 | 1 |
```

We fill in the boxes by reading the transitions from the transition diagram.

Similarly, for flip-flop B, we get:

```
B: 0 | 0 | 0 | 0 | 0 | 0 |
   0 | 0 | 0 | 1 | 1 | 1 |
```

Step II:
We now translate these transition maps to Karnaugh maps for the flip-flop inputs by using the properties of the flip-flop used. For a JK flip-flop,

- J must be 1 for $A$,
- we don't care what J is for $\beta$, 0, $X$,
- and J must be 0 for $B$.
- K must be 1 for $A$,
- we don't care what K is for 0, 0, $X$,
- and K must be 0 for $B$.

These are summarized in the "input equations" for the flip-flop discussed in Peterson, The Design of Digital Systems, Fig. 5-7.

For a JK flip-flop, we have:

- $J = \alpha$
- $DC_j = \beta$, 0, $X$
- $K = \beta$
- $DC_K = 0, 0, X$

(transitions where $J$ must equal 1)
(transitions for which we don't care what $J$ is)
($J = 0$ otherwise)
(similarly for $K$)

We use these to perform the translation of the transition maps to Karnaugh maps for the four inputs:

- $J_{A} = Q_{A B D}$
- $J_{B} = DQ_{A}$
- $K_{A} = DQ_{B}$
- $K_{B} = Q_{A D}$

(Note that it is easier to implement the complement of $K_A$ and $K_B$ than invert to get the desired fcn.)
Finally, we have \( E = D \overline{Q}_A \overline{Q}_B \).

This is the resulting circuit!

The clock inputs are both connected to the clock signal.

This circuit would be called a synchronous self-starting modulo three counter with carry output and count enable.

For further study: Figure out the input equations for D or T flip-flops. Design a counter using these instead of JK flip-flops.


Further input equations for D flip:

\[
\begin{align*}
D & \text{ must be } 1 \text{ for } a, 1 \\
\text{ only "don't care" condition is } & x
\end{align*}
\]

\[
\begin{align*}
D &= a, 1 \text{ (i.e., } 1 \text{ for } a, 1) \\
\overline{D} &= x \\
(D = 0 \text{ otherwise})
\end{align*}
\]

For T flip:

\[
\begin{align*}
T & \text{ must be } 1 \text{ for } a, \beta \\
\text{ only "don't care" condition is } & x
\end{align*}
\]

\[
\begin{align*}
T &= a, \beta \text{ (i.e., } T=1 \text{ for } a, \beta) \\
\overline{T} &= x \\
(T = 0 \text{ otherwise})
\end{align*}
\]