3. Analyze the operation of the following circuit:

The box represents a 4-bit synchronous binary counter. The clock runs at a continuous 100 kHz rate. The clock input is asynchronous.

(a) Suppose the input remains low for a long time. In what state will the counter eventually remain? What will be the state of the output?

(b) Now suppose a 1 as a positive pulse arrives at the input (sufficient to reset the counter). What happens now? What is the minimum length of the input pulse? (Explain)

(c) What happens if a second input pulse arrives while the output is high?

(d) Can there be "glitches" on the output pulse? (Explain why or why not)

Assume the counter is initially reset to 0 when the power is first turned on.
Consider the following state diagram:

There is one input (C) and no outputs. The circuit goes to state 11 when the input is high for three or more successive clock pulses. It can be used to detect a sequence of three or more 1's in an input data stream by decoding the state 11. The circuit is to be implemented using two JK flip-flops plus combinatorial circuitry as indicated below. Design the combinatorial circuits for Jk and Kk. Be reasonable efficient.

Skeleton of circuit: (combinatorial circuitry not shown)

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Extra Credit Problem

Below is a circuit for a dual-ramp ADC.

(a) Explain how it works, including a sketch of waveforms at the integrator output and the comparator output.

(b) What advantages does this design have for use in a low-cost digital voltmeter?

(c) Do you think such a design would be practical for CD recording where a digitization to 16 bit accuracy must be made every 23 μs? Explain briefly.

Figure from
Borna and Pover
Integrated Circuits in Digital Electronics
Wiley ©1973
2. (a) The counter is initially 0. It counts up until \(Q_1\) and \(Q_2\) are both 1, at which point the count enable (active low) input goes to 1 and further counting is disabled. Thus, the counter is in the state 010 = "6" and the output is 1, 1 = 0.

(b) The counter is reset to zero, so count enable = 0 and remains 0 at the clock transitions until the state "6" is reached. During this time the output is high. The minimum length of the output pulse is slightly more than 5 clock cycles (the clear input must arrive slightly before the clock transition for an immediate 0 → 1 transition of the counter). Then there are 5 full states (1, 2, 3, 4, 5). On the sixth clock edge, the reaches 6, the output goes low and counting stops.

Output  |
---|---
Input  |
Clock  |
Counter State | 6 → 5 → 4 → 3 → 2 → 1 → 0 → 6...

Min. output pulse width = 5 × 10 ns = 50 ns.
2 (continued)

(5) The output pulse is extended to 3 times
    after the second pulse (second input resets the
    counter to 0).

(6) Yes - for example, in the transition
    from 011 to 100, the 110 state can
    momentarily appear and result in a
    glitch (toward 0) of the output pulse.
    (This will not affect the count sequence
    since the glitch is momentary (!) and does
    not come during the setup time for the
    clock enable input. A glitch on the Clear
    input is another story).
4. The gating in the clock circuit allows the clock to get through to the counter only when the comparator output is “HIGH” (input < input). Assume the circuit starts with V+ only slightly greater than V-, so no clock pulse is generated by the comparator (we will see it is left in this state at the end of digitization).

To measure a voltage, S1 is closed and the counter is reset. Note that the on input is a virtual ground. \( I = -\frac{V_{in}}{R} \) flows through R (current flows to left) and the op amp output rises. This immediately changes the state of the comparator \((V_+ > V_-)\) so the counter starts counting. It continues and eventually the switch is set. This causes the switch driver to open S3 and close S2, \( V_+ > V_{in} \), and the current flows in the opposite direction:

\[ I = \frac{V_{in}}{R} \]

The integrator output now starts falling, and the lower order bits of the counter start again from zero. Eventually, the integrator output crosses zero and the clock stops. The number contained in the lower order bits (all our way which is \( V_{in} \)) is proportional to \( V_{in} \).

The comparator input is slightly less than the input, as we assumed at the beginning.

The waveform at the integrator and comparator outputs looks like:

\[ V(t) \quad \text{slope} = \frac{dV}{dt} = -\frac{1}{C} \frac{V_{in}}{R} \]

\[ \text{Integrator output} \]

\[ V(t) \quad \text{slope} = -\frac{1}{C} \frac{V_{R}}{R} \]

\[ V_m = V_{in} \frac{t_1}{R} \]

\[ V_0 = V_{R} \frac{t_2}{R} \]

\[ \Rightarrow V_{in} = V_R \frac{t_2}{t_1} \]

\[ \text{Comparator output} \]

\[ V_{in} = V_R \frac{t_2}{t_1} = V_R \frac{N_2/f_{\text{clock}}}{N_1/f_{\text{clock}}} = V_R \frac{N_2}{N_1} \text{ (fixed)} \]

\[ = V_{in} \cdot N_2 \text{ and all circuit element values cancel except } V_R. \]

This is an advantage to keep cost down (almost no critical component values).

(c) The maximum time for digitization (assuming you use only an ADC clock) can be very large for 11 bits of digitization, \( 2 \times 2^n \) clock periods for a maximum signal input. For 16 bits, this corresponds to 1.31x10^10 counts. This must be done in 23 ms, so for 1.31x10^10 counts \( \frac{23 \text{ ms}}{23 \text{ ms}} = 5.7 \text{ GHz} \) minimum.

This is not practical.