1. Assume that the output voltage limits are $0 \pm 15\text{V}$ for the op-amp.

(a) Find $V_+$ and $V_{out}$ when $V_{in} = -15\text{V}$.
(b) $V_{in}$ is now increased toward $+15\text{V}$. Find the threshold voltage for the output voltage to change and the new output voltage after the threshold is crossed.
(c) Explain why the output voltage changes rapidly after the threshold is crossed.
(d) Sketch the curve of $V_{out}$ vs. $V_{in}$ over the range of $V_{in}$ between $-15\text{V}$ and $+15\text{V}$, for $V_{in}$ both increasing and decreasing. (i.e., sketch the transfer characteristic). Explain what is meant by hysteresis.

2. A pulse, $V_{in} = V_0 (1 - e^{-at}) u(t)$, is input to the RC circuit shown. $R$ and $C$ for the networks are chosen such that $\frac{1}{RC} = a$. Refer to the table of Laplace transforms.
(a) Find $H(s)$ for the network.
(b) Find $\hat{V}_{in}(s)$.
(c) Find $\hat{V}_{out}(s)$, assuming the voltages and currents are zero for $t < 0$.
(d) Find $V_{out}(t)$. 
15. 3. (a) Write down the logical function, \( F(\overline{A}, B) \), implemented by the circuit above. (i.e., just transcribe the circuit diagram into a logical expression).

(b) Use theorems of Boolean algebra to simplify the expression.

(c) Implement the simplified expression using nands and inverters.

(d) Can this be implemented using a single 7400 chip (quad 2-input nand)? If so, how?

15. 4. (a) Make a Karnaugh map of the function:
\[ F(A, B, C) = \overline{A}BC + \overline{A}BC + A\overline{B}C + ABC \]

(b) Use the Karnaugh map to simplify the function.

(c) Could this be implemented using a single, fairly common gate?

15. 5. Simplify the function in the Karnaugh map below. Express the function in simplified sum-of-products form and implement with nands and inverters.

\[ f: \begin{array}{c|c|c|c|c|c|c}
A & B & C & f \\
00 & 01 & 11 & 10 & 0 & 1 & 1 \\
01 & 11 & 11 & 11 & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & & &
\end{array} \]

\[ \text{can use} \]
\[ 3\text{-input nands} \]
This is a diode-transistor logic (DTL) gate. Assume that the diodes have a forward voltage drop of 0.7 V and require more than 0.5 V forward bias for substantial current to flow.

(a) Let \( V_A = +5 \text{ V} \) and \( V_B = +5 \text{ V} \) (both inputs "true"). This means \( D_1 \) and \( D_2 \) are both reverse biased and current flows through \( R_1 \), \( D_3 \) and \( D_4 \) to pull up the voltage, \( V_o \), on the base of \( Q_1 \). Assume this is sufficient to bring the silicon BJT into saturation. Estimate \( V_2 \) and \( V_{out} \).

(b) Now set \( V_A = +5 \text{ V} \) (true) and \( V_B = +0.2 \text{ V} \) ("false"). Note that \( D_2 \) is now forward biased.

Estimate \( V_4 \), \( V_2 \) and \( V_{out} \).

(c) Assuming "true" = 5 V and "false" = 0.2 V make a truth table for this gate and see if you can recognize the logical function it performs.

**Hint:** Can \( D_3 \) and \( D_4 \) conduct appreciable current given your value of \( V_4 \)?
<table>
<thead>
<tr>
<th>( f(t) )</th>
<th>Property</th>
<th>( F(s) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Definition</td>
<td>( \int_0^\infty f(t)e^{-st} , dt )</td>
<td></td>
</tr>
<tr>
<td>Linearity</td>
<td>( F(s) + F_A(s) )</td>
<td></td>
</tr>
<tr>
<td>Linearity</td>
<td>( sF(s) )</td>
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<tr>
<td>Differentiation</td>
<td>( sF(s) - f(0) )</td>
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<tr>
<td>Differentiation</td>
<td>( sF(s) - f(0) - \frac{df(0)}{dt} )</td>
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</tr>
<tr>
<td>Integration</td>
<td>( \frac{1}{s} F(s) )</td>
<td></td>
</tr>
<tr>
<td>Complex differentiation</td>
<td>( \frac{dF(s)}{ds} )</td>
<td></td>
</tr>
<tr>
<td>Complex translation</td>
<td>( F(s + a) )</td>
<td></td>
</tr>
<tr>
<td>Real translation</td>
<td>( e^{-as}F(s) )</td>
<td></td>
</tr>
<tr>
<td>( \frac{1}{s} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \frac{1}{s+a} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \frac{1}{s^2 + \beta^2} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \frac{\beta}{s^2 + \beta^2} )</td>
<td></td>
<td></td>
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<tr>
<td>( \frac{s + a}{(s + a)^2 + \beta^2} )</td>
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<tr>
<td>( \frac{\beta}{(s + a)^2 + \beta^2} )</td>
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<tr>
<td>( \frac{1}{s^2} )</td>
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<tr>
<td>( \frac{1}{(s + a)^2} )</td>
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<tr>
<td>( \frac{1}{s^{n+1}} )</td>
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<td></td>
</tr>
<tr>
<td>( \frac{\alpha}{\bar{3}(s + \alpha)} )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\( V_R(t) = R \frac{d}{dt} I(t) \) \[ \Rightarrow \hat{V}_R(s) = R \hat{I}_R(s) \]

\( V_L(t) = \frac{1}{L} \int_0^t I_L(t') \, dt' \) \[ \Rightarrow \hat{V}_L(s) = \frac{1}{sL} \hat{I}_L(s) \]

\( V_C(t) = \frac{1}{C} \int_0^t E_C(t') \, dt' \) \[ \Rightarrow \hat{V}_C(s) = \frac{1}{sC} \hat{E}_C(s) \]

\( V_L(t) = \frac{d}{dt} I_L(t) \) \[ \Rightarrow \hat{V}_L(s) = sL \hat{I}_L(s) \]

**Note:** These equations require
\( V_L = 0 \) for \( t < 0 \) (a)
\( I_L = 0 \) for \( t < 0 \) (a)
(a) If $V_{in} = -15V$ and $V_{out} = +15V$,

$$V_+ = -15V + \frac{10k}{10k+15k} \times 30V = -3V < V_{=0V}$$

Contradiction $\implies V_{out} = -15V$.

$\therefore V_+ = -15V$.

(b) Threshold when $V_+ = 0V$, $V_{out} = -15V$.

\[
\text{I} = \frac{15V}{15k} = 1mA
\]

$\therefore V_{in} = 1mA \times 10k = 10V$.

(c) When the threshold is crossed, $V_{out}$ increases toward $+15V$. But this increases $V_+$ through the 15k feedback resistor, making the output increase all the more. $\implies$ positive feedback.

(d) Hysterisis: threshold for the transition is greater than threshold for -ve transition, leading to a two-valued transfer function between $-10V$ and $+10V$ for $V_{in}$. 

\[V_{out}
\]

\[\begin{array}{c|c|c|c|c}
-15 & & & -10 & V_{in} \\
\hline
 & -10 & & & +10 \\
\hline
 & & -15 & & \\
\end{array}\]
20.
\[ H(s) = \frac{R}{R + \frac{1}{RC}} = \frac{s}{s + \frac{1}{RC}} = \frac{s}{s + \frac{1}{\tau}} \quad \text{where} \quad \tau = \frac{1}{RC}. \]

(b) From table, \[ \hat{V}_{in}(s) = \frac{V_{0}A}{s(\tau + s)}. \]

(c) \[ \hat{V}_{out}(s) = H(s) \hat{V}_{in}(s) = \frac{V_{0}A}{s^{2}(\tau + s)} = \frac{V_{0}A}{s^{2}(s + \frac{1}{\tau})}. \]

(d) \[ \hat{V}_{out}(t) = V_{0}e^{-\frac{t}{\tau}} u(t) \]

\[ = \frac{V_{0}}{RC} e^{-\frac{t}{\tau RC}} u(t). \]

3.(a) \[ F = \overline{A \overline{B} \cdot \overline{A B}} \]

(b) \[ = A \overline{B} + A B \quad \text{(DeMorgan)} \]

\[ = A \overline{B} + \overline{A} B + A B + \overline{A} B \]

\[ = A (\overline{B} + B) + (A + \overline{A}) B = A + B \quad \text{(or could recognize immediately)} \]

\[ \overline{A \overline{B} + A B} = A + B \]

(c) \[ A + B = \overline{A \overline{B}} \]

(d) Yes, use two nands as inverters, so 2 of the 4 gates are used.

4.(a) \[ E = \begin{array}{c|c|c|c|c}
0 & 0 & 0 & 1 & 0 \\
0 & 1 & 0 & 1 & 0 \\
1 & 1 & 0 & 1 & 0 \\
1 & 0 & 0 & 0 & 1 \\
1 & 0 & 1 & 1 & 0 \\
1 & 1 & 0 & 0 & 1 \\
0 & 1 & 0 & 0 & 0 \\
1 & 0 & 1 & 0 & 0
\end{array} \]

(b) \[ F = \overline{A} C + A \overline{C} = A \overline{B} C \]

(c) \[ F = A \overline{C} + \overline{A} \overline{B} C \]
(a) \( R_1 \) is saturated so \( V_{BE} = 0.8 \text{V}, \quad V_{CE} = 0.2 \text{V} \)
\[ V_i = V_{BE} = 0.8 \text{V}, \quad V_{out} = V_{CE} = 0.2 \text{V}. \]

(b) \( D_2 \) is forward biased so \( V_i = 0.7 \text{V} + 0.2 \text{V} = 0.9 \text{V} \)
At least 1.0 V would be required for significant current to flow through \( R_2 \) in parallel with the BE diode. Thus \( V_i = 0 \text{V} \) and \( Q_2 \) is cut off so \( V_{out} = 5 \text{V}. \)

(c) \[
\begin{array}{c|c|c}
A & B & F \\
\hline
0 & 0 & 1 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]
\[ F = \overline{AB} \quad \text{(NAND)} \]